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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,626	HAKIM ET AL.	
	Examiner	Art Unit	
	Samir A. Ahmed	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-31,34-47,49-74 and 77-87* is/are rejected.

7)☐ Claim(s) *5,32,33,48,75 and 76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/1/04 has been entered.

2. The amendment filed 1/30/06 have been entered and made of record.

3. Applicant's arguments with respect to claims 1-87 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant alleges, "However, nothing in Neubauer shows [,]" (page 20, lines 8-10). The Examiner disagrees. The Examiner cannot find anywhere in the claim language of claims 1 and 44 the language "modifying first image data using at least some image data for an optical characteristic that is different from the first image data". While the claims recite "obtaining a second image data including at least some image data for an optical characteristic that is different from said first image data; and modifying said first image data by employing said second data", the claims do not recite "modifying first image data using at least some image data for an optical characteristic that is different from the first image data". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., modifying first image data using at least some image data for an optical characteristic that is different from the first image data) are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "29" in Fig. 1 has been used to designate both the "high-sure/low-sure image output from enhancer 28" and the "enhanced representation from representation generator 24". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 26-28, 69-71 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 26, recites, "applying said enhanced contrast representation to a third representation of the electrical circuit to provide an enhanced inspection representation for use in inspecting said electrical circuit for defects" on lines 8-10. While the specification as originally filed is enabling for applying the enhanced contrast representation 146 in Fig. 3 to the output of a third image (red image) of the circuit board convolved with a Laplacian of a Gaussian function 162 in Fig. 3 to provide an enhanced representation 29 for use in inspection, the specification as originally filed is not enabling for any third representation of the electrical circuit as recited in the claim. The third image representation of the electrical circuit could be the red image of the electrical board, a third image of a reference electrical circuit corresponds to the electrical circuit inspected or an enhanced third image enhanced by convolution with any function other than Laplacian function or enhanced by any other way other than convolution. The specification as originally filed only discloses an embodiment shown in Fig.3 that discloses, applying the enhanced contrast representation 146 in Fig. 3 to the output of a third image (red image) of the circuit board convolved with a Laplacian of a Gaussian function 162 in Fig. 3 to provide an enhanced representation 29 for use in inspection. Nowhere in the original specification, an embodiment that discloses any of the other third representations of the electrical circuit outlined above exits.

As to claim 69 refer to claim 26 rejection.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1- 4, 6-25, 31, 34-47, 49-68, 74, 77-87 are rejected under 35 U.S.C. 102(a) as being anticipated by Kaminsky, Roland et al. (WO 00/11454).

As to claims 1 and 44, Kaminsky discloses a method of inspecting electrical circuits comprising:

obtaining first image data relating to at least a part of an electrical circuit [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), any image for example R image is a first image];

obtaining second image data generally corresponding to said part of an electrical circuit, said second image data including at least some image data for an optical characteristic that is different from said first image data [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), G image is a second image that represents reflections in a different wavelength (optical characteristic that is different from said first image)];

modifying said first image data by employing said second image data thereby to produce an enhanced representation of the electrical circuit [combining the three colors (i.e., modifying the first image by using the second image) using a matrix shown in page 6, lines 10-13 to produce an enhanced representation of the PCB that distinguishes the

existence of oxide from laminate and copper on the PCB. Also PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21 discloses generating three color images R, G, B of the PCB and a composite (combined) "gray level" reflection value is generated by weighting the measured intensities of the three colors (optical characteristics of the R, G, B images) to give an optimum contrast between the metal and bare substrate of the PCB (PCT/IL98/00285, page 14, lines 5-19), i.e., the weighted combining of the first and second images results in an enhanced image); and

inspecting the enhanced representation with reference to a reference representation of the electrical circuit to detect defects in the electrical circuit [during testing (inspection), a comparison between the image and reference sample of oxide is performed to detect the presence of oxide (defect) (page 8, last line-page 9, line 2). Also PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21 discloses using a reference representation for comparison to detect defects (page 21, lines 13-16)].

As to claims 2 and 45, Kaminsky further discloses, wherein said first image data is in a first spectral range and second image data includes at least some image data in a second spectral range (page5, line21).

As to claims 3, 6, 46 and 49, Kaminsky further discloses enhancing contrast between at least some parts of said second image data representing corresponding parts of the electrical circuit represent [to define a "low sure" threshold for pixels near transition between conductor and laminate, calculation detailed in Fig. 15 from US

Patent 5,774,573 (Caspi et al.) is used to enhance contrast between image data corresponding to conductor and laminate (parts of electrical circuit) on the PCB (page 5, line 32-page 6, line 5). Caspi et al. is incorporated by reference in Kaminsky (page 1, lines 16-17)].

As to claims 4, 7, 47 and 50, Kaminsky further discloses, wherein said enhancing contrast is non-linear [the matrix cited on page 6, lines 10-13 and shows the enhanced gray level contrast is non-linear. Also PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21) discloses generating three color images R, G, B of the PCB and a composite (combined) "gray level" reflection value is generated by weighting the measured intensities of the three colors (optical characteristics of the R, G, B images) to give an optimum contrast between the metal and bare substrate of the PCB (PCT/IL98/00285, page 14, lines 5-19). This transformation of pixel intensity values by assigning different weights to pixel intensity values of different regions of the image to produce an optimum contrast between these regions is non-linear transformation, because by doing so the different portions of the image are not transformed proportionally (linearly). Also Fig. 15 from US Patent 5,774,573 (Caspi et al.) is used to enhance contrast between image data corresponding to conductor and laminate (parts of electrical circuit) on the PCB (page 5, line 32-page 6, line 5) and as disclosed in Caspi (col. 8, lines 7-11), the convolution is performed by a second derivative of a Gaussian function (non-linear enhancing contrast). Caspi et al. is incorporated by reference in Kaminsky (page 1, lines 16-17)]

As to claim 8, 11, 51, and 54, Kaminsky further discloses, convolving said first image data With a function) [Fig. 15 from US Patent 5,774,573 (Caspi et al.) is used to enhance contrast between image data corresponding to conductor and laminate (parts of electrical circuit) on the PCB (page 5, line 32-page 6, line 5) and as disclosed in Caspi (col. 8, lines 7-11), the convolution is performed by a second derivative of a Gaussian function. Caspi et al. is incorporated by reference in Kaminsky (page 1, lines 16-17)].

As to claims 9, 12, 52, and 55, Kaminsky further discloses, wherein said function is an approximation of a Laplacian of a Gaussian function [Fig. 15 from US Patent 5,774,573 (Caspi et al.) is used to enhance contrast between image data corresponding to conductor and laminate (parts of electrical circuit) on the PCB (page 5, line 32-page 6, line 5) and as disclosed in Caspi (col. 8, lines 7-11), the convolution is performed by a second derivative of a Gaussian function. Caspi et al. is incorporated by reference in Kaminsky (page 1, lines 16-17)].

As to claims 10, 13, 53, and 56, Kaminsky further discloses, wherein said modifying is carried out following said convolving [the convolution disclosed in Fig 15. from US Patent 5,774,573 (Caspi et al.) is used to enhance contrast between image data corresponding to conductor and laminate (page 5, line 32-page 6, line 5) and the matrix (modifying) is generated after that (page 6, lines 8-13)].

As to claim 14, 57, Kaminsky further discloses,

determining in said first image data approximate locations of transitions between image regions having distinguishable optical characteristics [Caspi et al. incorporated by

reference in Kaminsky (page 1, lines 16-17) further discloses determining transitions between edges (image regions having distinguishable optical characteristics) in the image (col. 13, lines 45-59)]; and wherein

said modifying comprises removing undesired ones of said transitions [Caspi discloses classifying the identified transition pixels as either white or black to eliminate the abrupt transition regions between edges (col.13, line 60-col.14, line 10)].

As to claims 15, 20, 58 and 63, Kaminsky further discloses, wherein said enhanced representation is a binary representation of said electrical circuit [Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses, black and white (binary) representation of the PCB (col. 13, lines 45-52)].

As to claims 16, 21, 59, and 64, Kaminsky further discloses, wherein said enhanced representation is a representation of contours in said electrical circuit, which indicate approximate locations of transitions between regions in said electrical circuit exhibiting distinguishable optical characteristics [Fig 15 from US Patent 5,774,573 (Caspi et al.) used to enhance contrast between image data corresponding to conductor and laminate (page 5, line 32-page 6, line 5), shows that the enhanced representation is a contour (distinguishable optical characteristic) in the PCB (Caspi, Fig.15, step 327, col.16, lines 7-25)].

As to claims 17, 22, 60 and 65, Kaminsky further discloses, wherein said enhanced representation has a spatial resolution that is greater than the spatial resolution of said first and second image data [Caspi et al. incorporated by reference in

Kaminsky (page 1, lines 16-17) further discloses the enhanced image has a higher resolution than the original image (col.2, line66-col. 3, line 16)].

As to claims 18, 23, 61, and 66, Kaminsky further discloses, wherein said enhanced representation has a gray scale whose dynamic range is reduced as compared with the dynamic range of a gray scale of said first and second image data [Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses. enhanced representation has a gray scale whose dynamic range is reduced as compared with the dynamic range of a gray scale of the original image data (col. 13, lines 6-59)].

As to claims 19, and 62, Kaminsky further discloses,

determining in said first image data approximate locations of transitions between image regions having distinguishable optical characteristics [Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses determining transitions between edges (image regions having distinguishable optical characteristics) in the image (col. 13, lines 45-59); and wherein

said modifying includes overriding at least part of said convolved first image [Caspi discloses classifying the identified transition pixels as either white or black to eliminate the abrupt transition regions between edges in the convolved image (col.16, lines 7-43)].

As to claims 24, and 67, Kaminsky further discloses, wherein said first and second images are acquired with at least one imager comprising at least two different types of optical detectors arranged to view at least a portion of said electrical circuit

illuminated by at least one illuminator [PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21) discloses an optical array 260 to generate the three colored images, includes three illuminator units 10 (at least one illuminator), each unit includes separate collecting optics (detectors) 24 (fig.1). Each of CCD lines 25-27 includes a line of detectors. The separate collector optics image a linear segment of the workpiece (PCB) surface onto one of the sections of line detectors 25-27. The three CCD lines 25-27 (at least one imager) each represent Red, Green, and Blue color spectrums respectively (at least two different types of optical detectors (page 19, line 30-page 20, line 5, Figs. 1 and 6)].

As to claims 25, and 68, Kaminsky further discloses, wherein said first and second images are generally spatially coincidental, and each of said first and second images are in a different spectral range [PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21) discloses the respective fields of view of the collector optics (detectors) overlap and the three CCD lines 25-27 each represent Red, Green, and Blue color spectrums respectively, and are offset such that they image slightly offset lines on the illuminated portion of the work piece (PCB)(page 19, line 34-page 20, line 10) (i.e., first and second images are slightly offset (generally spatially coincident) and at red, green and blue spectrums (different spectral ranges)].

As to claims 31, and 74, Kaminsky discloses a method of inspecting electrical circuits comprising:

obtaining first image data relating to at least a part of an electrical circuit [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), any image for example R image is a first image];

obtaining second image data relating to said at least part of an electrical circuit [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), G image is a second image];

non-linearly combining said first image data and said second image data to form pseudo image [PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21) discloses generating three color images R, G, B of the PCB and a composite (combined) "gray level" reflection value is generated by weighting the measured intensities of the three colors (optical characteristics of the R, G, B images) to give an optimum contrast between the metal and bare substrate of the PCB (PCT/IL98/00285, page 14, lines 5-19). This transformation of pixel intensity values by assigning different weights to pixel intensity values of different regions of the image to produce an optimum contrast between these regions is non-linear transformation, because by doing so the different portions of the image are not transformed proportionally (linearly), the combined image is a pseudo image], and supplying said pseudo-image to a high-sure/low-sure region classifier [the image is supplied to low-sure/high-sure circuit detailed in Fig. 15 from US Patent 5,774,573 (Caspi et al.), which is incorporated by reference in Kaminsky (page 1, lines 16-17) to determine a threshold to classify the image (page 5, line 32-page 6, line 5)].

As to claims 34 and 77, Kaminsky further discloses, wherein said high-sure/low-sure classifier operates on the pseudo image to produce a high-sure/low-sure image output including at least three regions:

(i) a low-sure region that to a high degree of confidence represents only substrate;

(ii) a high-sure region that to a high degree of confidence represents only conductor located on the top surface of said electrical circuit; and

(iii) a third region which is neither high-sure nor low-sure [Fig. 15 from US Patent 5,774,573 (Caspi et al.), which is incorporated by reference in Kaminsky (page 1, lines 16-17) and used to determine a threshold to classify the image (Kaminsky, page 5, line 32-page 6, line 5) and (Caspi, col. 16, lines 1-61, col. 18, lines 14-63, Fig.20)].

As to claim 35, Kaminsky further discloses, further comprising:

receiving said first image data and employing said high-sure/low-sure image to selectively modify an interim image formed from said first image data to produce an enhanced representation of said electrical circuit [US Patent 5,774,573 (Caspi et al.), which is incorporated by reference in Kaminsky (page 1, lines 16-17) and used to determine a threshold to classify the image (Kaminsky, page 5, line 32-page 6, line 5) discloses employing a high-sure/low-sure image to selectively modify an interim image formed from the first image (col. 18, lines 47-56)].

As to claims 78 and 79, Kaminsky further discloses, further comprising:

a representation generator receiving said first image data, said representation

generator including an override circuit in communication with said high-sure/low-sure classifier and operative to employ said high-sure/low-sure image to selectively modify image data being processed in said representation generator to produce an enhanced representation of said electrical circuit; and wherein said representation generator is operative to process said first image data [US Patent 5,774,573 (Caspi et al.), which is incorporated by reference in Kaminsky (page 1, lines 16-17) and used to determine a threshold to classify the image (Kaminsky, page 5, line 32-page 6, line 5) discloses employing a high-sure/low-sure image to modify the image by removing abruptly transitions (overriding part of the output image from the high-sure/low-sure classifier) (col.16, lines 7-56)].

As to claims 36 and 80, Kaminsky further discloses, further comprising:

convolving said first image data with a mathematical function approximating 2-dimensional Laplacian of a Gaussian function [Caspi et al. is incorporated by reference in Kaminsky (page 1, lines 16-17) and Fig. 15 is used for convolving the image with a 2D Laplacian of a Gaussian function (Caspi, (col. 8, lines 7-11)].

As to claims 37 and 81, Kaminsky further discloses,

determining in said first image data approximate locations of transitions between image regions having distinguishable optical characteristics [Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses determining transitions between edges (image regions having distinguishable optical characteristics) in the image (col. 13, lines 45-59)].

As to claims 38 and 82, Kaminsky further discloses, wherein said enhanced representation is a binary representation of said electrical circuit [Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses, black and white (binary) representation of the PCB (col. 13, lines 45-52)].

As to claims 39 and 83, Kaminsky further discloses, wherein said enhanced representation is a representation of contours in said electrical circuit, which indicate approximate locations of transitions between regions in said electrical circuit exhibiting distinguishable optical characteristics [Fig 15 from US Patent 5,774,573 (Caspi et al.) used to enhance contrast between image data corresponding to conductor and laminate (page 5, line 32-page 6, line 5), shows that the enhanced representation is a contour (distinguishable optical characteristic) in the PCB (Caspi, Fig.15, step 327, col.16, lines 7-25)].

As to claims 40 and 84, refer to claim 39, 83 rejections above. Caspi further discloses detects transitions between substrate and conductors on a top surface (Fig.5) and eliminate transitions between substrate and conductors (Fig. 6, item 16)].

As to claims 41 and 85, Kaminsky further discloses, further comprising:

analyzing said enhanced representation to provide an indication of defects in said electrical circuit [[during testing (inspection), a comparison between the image and reference sample of oxide is performed to detect the presence of oxide (defect) (page 8, last line-page 9, line 2). Also PCT/IL98/00285 used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21 discloses using a reference representation for comparison to detect defects (page 21, lines 13-16)].

As to claims 42 and 86 refer to claim 24 and 67 rejections.

As to claims 43 and 87 refer to claim 25 and 68 rejections.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 26-27 and 69-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kaminsky, Roland et al. (WO 00/11454) and Colvin (US Patent 5,970,167).

As to claims 26 and 69 [As best understood by the Examiner], Kaminsky discloses a method of inspecting electrical circuits comprising:

obtaining first image data relating to at least a part of an electrical circuit in at least first spectral range [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), any image for example R image is a first image in a first spectral range];

obtaining second image data relating to at least part of an electrical circuit in at least second spectral range [three color images R, G, B images are generated for the PCB (page 5, lines 11-21), G image is a second image in a second spectral range];

providing an enhanced contrast representation of the electrical circuit by non-linearly combining said first image data and said second image data [PCT/IL98/00285

used in the preferred embodiment of Kaminsky and incorporated by reference (see page 5, lines 11-21) discloses generating three color images R, G, B of the PCB and a composite (combined) "gray level" reflection value is generated by weighting the measured intensities of the three colors to give an optimum contrast between the metal and bare substrate of the PCB (enhanced contrast representation) (PCT/IL98/00285, page 14, lines 5-19). This transformation of pixel intensity values by assigning different weights to pixel intensity values of different regions of the image to produce an optimum contrast between these regions is non-linear transformation, because by doing so the different portions of the image are not transformed proportionally (linearly)]. Kaminsky does disclose, applying said enhanced contrast representation to a third representation of the electrical circuit to provide an enhanced inspection representation for use in inspecting said electrical circuit for defects.

Colvin discloses a method for analyzing failures in integrated circuits. A first image in a first channel of an RGB digitizer is obtained and a second image in a second channel of RGB digitizer is obtained. The first and second images are combined to produce an enhanced representation (col.6, lines 41-60). One of the three images of the RGB digitizer may obtained from an integrated circuit chip that is different from the integrated circuit used to obtain the other images (third representation of the electrical circuit).For example an image from an integrated circuit free from defects may be stored in the red channel (third representation of the electrical circuit) and images from the circuit board under test may be stored in each of the green and blue channels. When the image of the first integrated circuit stored in one channel of the RGB digitizer is

aligned with (applied to) the image of the second integrated stored in two channels of the RGB digitizer (enhanced contrast representation), the result is an image that shows any defects (provide an enhancement inspection representation for use in inspection) (col. 7, line 65-col.8, line 29). It would have been obvious to one of ordinary skill in the art at the time of the invention to use Colvin's teachings to modify Kaminsky's method by applying said enhanced contrast representation to a third representation of the electrical circuit to provide an enhanced inspection representation for use in inspecting said electrical circuit for defects in order to detect and highlight the exact location of a failure or defect in an integrated circuit.

As to claims 27 and 70, Kaminsky further discloses, wherein said enhanced contrast representation includes information providing enhanced contrast between representations of said first conductors and of said electrical circuit substrate [contrast is enhanced between metal (first conductor) and laminate (substrate) (page 2, lines 17-24; page 9, lines 1-7)] and Caspi et al. incorporated by reference in Kaminsky (page 1, lines 16-17) further discloses that conventional printed circuit boards comprises a non conductive substrate on one or both surfaces of which are deposited conductive tracks or lines (col. 1, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conventional teachings of Caspi to modify the combined method of Kaminsky and Colvin by using a printed circuit board having non-conductive substrate with conductive conductors on both sides, the modification would have been motivated by conventional reasons such as the wide spread usage of such printed circuit boards in electronic equipment because of their compactness, reduced

size and low cost that makes these printed circuit boards attractive for use in compact and portable small size electronic equipment.

12. Claims 28, and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kaminsky, Roland et al. (WO 00/11454) and Colvin (US Patent 5,970,167) as applied to claims 26 and 69 above and further in view of Bishop (US Patent 6,603,877).

As to claims 28 and 71, neither Kaminsky nor Colvin discloses, wherein said enhanced contrast representation exhibits decreased artifacts resulting from non-opaque characteristic of a substrate.

Bishop discloses an optical imaging system for determining different material regions on an object such as electronic circuit boards or wafers (col. 1, lines 8-16). An inspection of multilevel metal mask that contains a top metal surface and a bottom metal surface and holes through the material (col. 6, lines 23-32) is performed using two cameras, to distinguish holes from all other material by detecting the brightness of transmitted light (non-opaque characteristic of a substrate). As a result, holes image dark on top surface camera and bright on the bottom surface camera as shown in Figs. 12 and 13 (col. 7, lines 7-24). The two cameras imaging the surface using two different color filters (i.e., two images at two different spectral ranges are obtained), the output of the two cameras is combined (i.e., an enhanced contrast representation is generated)(see fig. 5, col. 4, lines 19-45). As shown in Fig. 25, the certainty image (enhanced contrast image), the artifacts in the ambiguity image (artifact image) shown in Fig. 26 is eliminated. It would have been obvious to one of ordinary skill in the art at

the time of the invention to use Bishop's teachings to modify the combined method of Kaminsky and Colvin by generating an enhanced contrast representation of the mask image that exhibits decreased artifacts resulting from non-opaque characteristic of the mask (substrate) in order to allow for a higher, more sophisticated and accurate level of optical inspection of printed circuit boards and provide a high degree of likelihood and lack of ambiguity of the material identification and characterization of several different regions of different image characteristics on the printed circuit board.

13. Claims 29-30, and 72-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Elyasaf et al. 6,175,645) and Bishop (US Patent 6,603,877).

As to claims 29 and 72, Elyasaf discloses a method of inspecting electrical circuits formed on different surfaces of a non-opaque substrate (Fig.1) comprising:

obtaining image data relating to at least part of an electrical circuit [a first image of the photomask is obtained at first light radiation (col.2, lines 30-42), the first light is at a different wavelength from a second light (col. 3, lines 35-40)], said electrical circuit being formed on both sides of a non-opaque substrate (col. 4, lines 37-43), said image data including artifacts resulting from a non-opaque characteristic of the substrate [image data contains defects in the form of variations of the transparent (artifacts resulting from the non-opaque substrate) and opaque regions (col. 4, lines 43-48). Elyasaf further discloses obtaining a second image of the photomask at a second light radiation (col. 2, lines 30-42), the second light illuminating the same portion of mask's face and at a different wavelength from that of the first light [i.e., different optical data for

an optical characteristic (second image data at second wave length) that is different from an optical characteristic of said image data (first image data at a first wavelength)].

Elyasaf does not disclose, enhancing said image data using different optical data for an optical characteristic that is different from an optical characteristic of said image data to provide enhanced inspection output information which decreases said artifacts in said image data.

Bishop discloses an optical imaging system for determining different material regions on an object such as electronic circuit boards or wafers (col. 1, lines 8-16). An inspection of multilevel metal mask that contains a top metal surface and a bottom metal surface and holes through the material (col. 6, lines 23-32) is performed using two cameras, to distinguish holes from all other material by detecting the brightness of transmitted light (non-opaque characteristic of a substrate). As a result, holes image dark on top surface camera and bright on the bottom surface camera as shown in Figs. 12 and 13 (col. 7, lines 7-24). The two cameras imaging the surface using two different color filters [i.e., two images first and second at two different spectral ranges (wavelengths) are obtained], the output of the two cameras is combined [i.e., the second image of the mask at a different spectral range (different optical data for an optical characteristic that is different from an optical characteristic of said image) is used to enhance the first image data at a first spectral range and produce an enhanced contrast representation] (see fig. 5, col. 4, lines 19-45). As shown in Fig. 25, the certainty image (enhanced contrast image), the artifacts in the ambiguity image (artifact image) shown in Fig. 26 is eliminated. It would have been obvious to one of ordinary

skill in the art at the time of the invention to use Bishop's teachings to modify the method of Elyasaf by combining second image of the mask at a different spectral range (different optical data for an optical characteristic that is different from an optical characteristic of said image) with the first image data of the mask to enhance first image data to provide enhanced inspection output information which decreases said artifacts in said image data in order to allow for a higher, more sophisticated and accurate level of optical inspection of printed circuit boards and provide a high degree of likelihood and lack of ambiguity of the material identification and characterization of several different regions of different image characteristics on the printed circuit board.

As claims 30 and 73, Elyasaf further discloses, wherein the electrical circuits comprise first conductors on a first side of the substrate and second conductors on a second side of the substrate, and the artifacts include at least part of an image from a substrate portion not having deposited thereon one of said first and second conductors (col. 4, lines 37-48).

Allowable Subject Matter

14. Claims 5, 32, 33, 48, 75, 76 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samir A. Ahmed whose telephone number is (571) 272-7413. The examiner can normally be reached on Mon-Fri 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (571) 272-7778. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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